#11/10-6-03 w Jony

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Harmer	Docket No:	TI-27445
Serial No:	09/374,079	Examiner:	Baker, S.
Filed:	08/12/99	Art Unit:	2133

For: ECC IN COMPUTER SYSTEM WITH ASSOCIATED MASS STORAGE DEVICE, AND METHOD FOR OPERATING SAME

APPEAL BRIEF PURSUANT TO 1.192(c)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the Final Rejection mailed December 31, 2002.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-26 were originally filed and Claims 11 and 13-26 have been cancelled. Thus, the subject matter of the instant Appeal is the final rejection of Claims 1-10 and 12.

STATUS OF AMENDMENTS

The application was originally filed with Claims 1-26. By virtue of an amendment filed on April 22, 2002, Appellants have cancelled Claims 13-26. Claims 7, 9, and 10 were amended. Additionally, by virtue of an amendment filed October 14, 2002, Claim 11 was cancelled. Further, a Response After Final was filed on March 7, 2003, amending no claims. No Advisory Action has been received by Applicants.

SUMMARY OF THE INVENTION

A block diagram of a computer environment in which the invention may be employed is shown in Figure 1. The computer environment includes a computer system 10 having a host computer 12, which includes, among other things, a CPU 14, a random access memory (RAM) 16, and various device drivers 18.

Associated with the host computer 12 is a mass data storage device 20.

A digital signal processor (DSP) 23 is typically employed to control the operation of the mass data storage device 20 and associated electronic circuitry.

The control of the data that is written to and read from the data media 22 is control by a control circuit 24 which contains the electronics necessary for the particular installation in which the mass data storage device 20 is employed.

Another environment in which the invention may be employed is that of the so-called RAID mass data storage array, as shown in the block diagram of Figure 2.

In the environment described above with respect to Figures 1 and 2, and in accordance with a preferred embodiment of the invention, at least some of the error correction coding (ECC) functions are removed from the mass data storage device 20 to be performed by the host computer 12. Preferably, the portions of the ECC functions that are performed by the host computer 12 are contained in the software or firmware of the device drivers 18. This enables the memory that formerly was used in performing the ECC functions of the control circuit 24 to be removed from the mass data storage device 20.

For a read operation, the user data is processed by the control electronics and firmware on the mass data storage device; however, the control electronics 24 only contains logic for performing error detection. There is no error correction capability in either the control electronics or the firmware on the mass storage device. Thus, a hardware circuit is provided on the mass data storage device 20 to check each sector of data that is read. If an error is found, the mass data storage device transfers to the device driver in the host for further processing both the uncorrected user data and the associated correction code for those sectors that have errors detected. Of course, the host now has an additional device driver capable of operating the mass data storage device 20. For sectors of user data in which the control electronics of the mass data storage device has detected an error, the device driver now corrects the user data, using the correction code for that sector.

The ECC functions are contained in the software of the device drivers. The drivers may be contained on the media of the disk and the software executed by the host CPU 14. Of course, the drivers may be contained in a memory of the host computer 12, and executed by the host CPU 14. In any event, the actual correction of

data read from the data storage medium 22 is performed by the host CPU 14, not by the DSP or CPU associated with the mass data storage device 20.

Thus, in operation, as data is written to the data storage medium 22, the ECC circuitry 25 generates or computes the parity or other error correction code signal to the associated drive 20 together with the data to be written to the data storage medium 22.

It will be appreciated that by relocation of the performance of the error correction steps to the host computer, and, more particularly, to the execution of the software of a device driver in the host computer, a significant number of advantages may be realized. For example, merely by removing the ECC memory from the mass data storage device 20, a significant savings in control circuitry contained in the mass data storage device can be realized. Further significant savings in the control circuitry is also realized by removing the correction functions, other than those of the initial error determination and ECC code generation described above. Furthermore, since the error correction process is determined by the software of the device drivers, which are control by the host CPU 14, the selection of any particular ECC technique that may be employed with respect to an associated mass data storage device can be easily changed more readily than if the entire ECC hardware of the mass data storage device had to be changed.

A flow chart of an embodiment of a software device driver that is executed in a host computer, together with the data flow paths resulting from the execution thereof, are shown in Figure 4.

ISSUES

The four issues on Appeal are first whether Claims 1, 3, 5, and 6 are anticipated under §102(e) by Nasu, second whether Claims 1-3 are anticipated under §102(e) by Hogan, third whether Claims 4, 7-10, and 12 are unpatentable under §103 over Nasu, and fourth whether Claims 4-9 and 12 are unpatentable under §103 over Hogan.

GROUPING OF THE CLAIMS

Each of Claims 1 and 7 as contained in the attached Appendix are independently patentable, and these rejected claims do not stand or fall together for the reasons more clearly set forth herein below.

ARGUMENTS

Nasu does not disclose or suggest the presently claimed invention including the device driver performing at least some ECC instructions in independent Claim 1.

The C1 correction unit and C2 syndrome calculator disclosed by Nasu do not relate to a device driver.

The definition of the device driver as supplied by the Examiner is a device specific control program that enables a computer to work with a particular device such as a disk driver.

Please note that the definition states a specific control program. What is it specific to? It is specific to the particular device and the computer.

There is no indication in Nasu that the C1 correction unit and the C2 syndrome calculator have any connection to the mass storage device. Without such a connection, C1 and C2 are not a device driver.

It is respectfully submitted that Nasu does not disclose or suggest the presently claimed invention including the facility for ECC instructions from a BIOS as defined in independent Claim 7.

The C1 correction unit and C2 syndrome calculator do not relate to a BIOS.

The Examiner alleges that official notice is given the advantages of placing the code for hard disk driver in system BIOS.

This allegation is traversed and a teaching from the prior art is requested.

Hogan does not disclose or suggest the presently claimed invention including the device driver for performing at least some ECC instructions in independent Claim 1.

The Examiner alleges that Hogan software instructions are apparently part of the disk device specific control program for enabling a computer to work with a disk device and thus can be seen to be part of the device driver.

Notwithstanding the allegations of the Examiner, Hogan does not disclose that the alleged software instructions have any connection to a device driver since Hogan does not disclose a device driver.

It is respectfully submitted that Hogan does not disclose or suggest the presently claimed invention including the facility for execution of ECC instructions from a BIOS as defined in independent Claim 7.

Applicants agree with the Examiner's evidence by page 6 of the Final Office Action that Hogan doesn't specify that the hard disk drive ECC decoding software instructions are in system BIOS.

The Examiner alleges that official notice is given to the advantages of placing the code for hard disk drive in system BIOS.

This allegation is respectfully traversed, and a teaching from the prior art is respectfully requested.

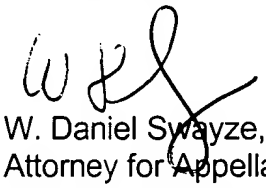
It is respectfully submitted that Claims 1-10 and 12 patentably define over the applied art.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-10 and 12 under 35 U.S.C. § 102 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

1. A computer system comprising:

a host computer having a CPU;

a mass data storage device associated with said host computer;

at least some ECC hardware associated with said mass data storage device;

and a device driver comprising software instructions for execution by said CPU for performing at least some ECC instructions on data read from said mass data storage device.

2. The computer system of claim 1 wherein said mass data storage device is a hard disk drive assembly.

3. The computer system of claim 1 wherein said host computer further comprises a RAM and wherein said at least some ECC instructions are performed upon read data contained in said RAM.

4. The computer system of claim 1 wherein said at least some ECC hardware associated with said mass data storage device includes hardware to generate data integrity determination information when a block of data is written to said mass data storage device.

5. The computer system of claim 1 wherein said at least some ECC hardware associated with said mass data storage device includes hardware to generate an error flag if an error is detected in said data read from said mass data storage device.

6. The computer system of claim 5 wherein said software instructions for execution by said CPU perform data correction on data read from said mass data storage device using said ECC code when said error flag has been generated.

7. A computer system comprising:

a mass data storage device containing a data medium and having associated ECC circuitry for generating an error flag indication of the occurrence of an error in data read from said data medium;

and a host computer having at least a RAM, a CPU, and a facility for executing ECC instructions from a BIOS by said CPU;

wherein execution of said ECC instructions corrects in said RAM data read from said medium according to said ECC codes when said error flag has been generated.

8. The computer system of claim 7 wherein said ECC instructions are software instructions of a device driver.

9. The computer system of claim 7 wherein said BIOS is a system BIOS.

10. The computer system of claim 7 wherein said BIOS is an expansion BIOS.

12. The computer system of claim 7 wherein said ECC circuitry determines the presence of an error in said read data from data integrity determination information previously generated from said read data.